

Application No. 10806041 (Docket: CNTR.2215)
37 CFR 1.111 Amendment dated 02/21/2007
Reply to Office Action of 11/22/2006

AMENDMENTS TO THE SPECIFICATION

Please delete the section entitled "SUMMARY OF THE INVENTION" in its entirety and substitute the following section therefor:

SUMMARY OF THE INVENTION

[0010] The present invention, among other applications, is directed to solving the above-noted problems and addresses other problems, disadvantages, and limitations of the prior art. The present invention provides a superior technique for enabling measured and graceful power management transitions in a computing device that allows for less stringent voltage surge compensation mechanisms to be employed in an associated power supply and within the computing device itself, resulting in systems that are less costly than have heretofore been provided. In one embodiment, an apparatus for providing measured power transitions in a computing device is envisioned. The apparatus includes power control logic and interval logic. The power control logic is that is configured to determine if the computing device is to enter a low power state. The power control logic has a logic generates plurality of stop signals, each sequentially indicating that a corresponding clock signal be stopped. The corresponding clock signal is operatively coupled to a corresponding sector logic element within the computing device. The interval logic is coupled to the power control logic, and is configured to provide a programmable number of clock cycles to the power control logic, whereby the power control logic causes the each of the plurality of stop signals to indicate that the corresponding clock signal be stopped after the programmable number of clock cycles.

[0011] One aspect of the present invention contemplates a power transition management mechanism. The power transition management mechanism has interval logic and power control logic. The interval logic provides one or more programmable numbers of clock cycles. The power control logic is coupled to the interval logic. The power control logic receives the one or more programmable numbers, and employs the one or more programmable numbers to sequentially stop each of a plurality of clock signals that are coupled to each of a corresponding plurality of sector logic elements.

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[0012] Another aspect of the present invention comprehends a method for providing measured power transitions in a computing device. The method includes determining if the computing device is to enter a low power state, ~~and sequentially~~ sequentially stopping clock signals that are coupled to each of a plurality of sector logic elements, and providing a programmable number of clock cycles that are to transpire between said stopping of the clock signals.